



**The Islamic University**  
**College of Technical Engineering**  
**Department of Computer Technical Engineering**



**Second Stage**

# ***Microprocessor Architecture***

**Lecture 7**

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# Contents

**The student will recognize the following Contents :**

➤ **Memory segmentation.**

# **Memory segmentation**

Segmentation provides a powerful memory management mechanism. It allows programmers to partition their programs into modules that operate independently of one another. Segment it is an area of memory that include up to 64K bytes and begins on an address evenly divisible by 16 and allow two processes to easily share data.

## **Concept of segmented memory**

- It allows the memory addressing capacity to be 1 Mbytes.
- It allows instruction code, the data stack and portion of the program to be more than 64KB longer.
- It facilitates the use of separate memory areas for program, data and stack.
- In this program can be relocated which is very useful in multiprogramming.
- It permits a program or its data to be put in different areas of memory.

# Memory segmentation

There are four segment register in 8086 :

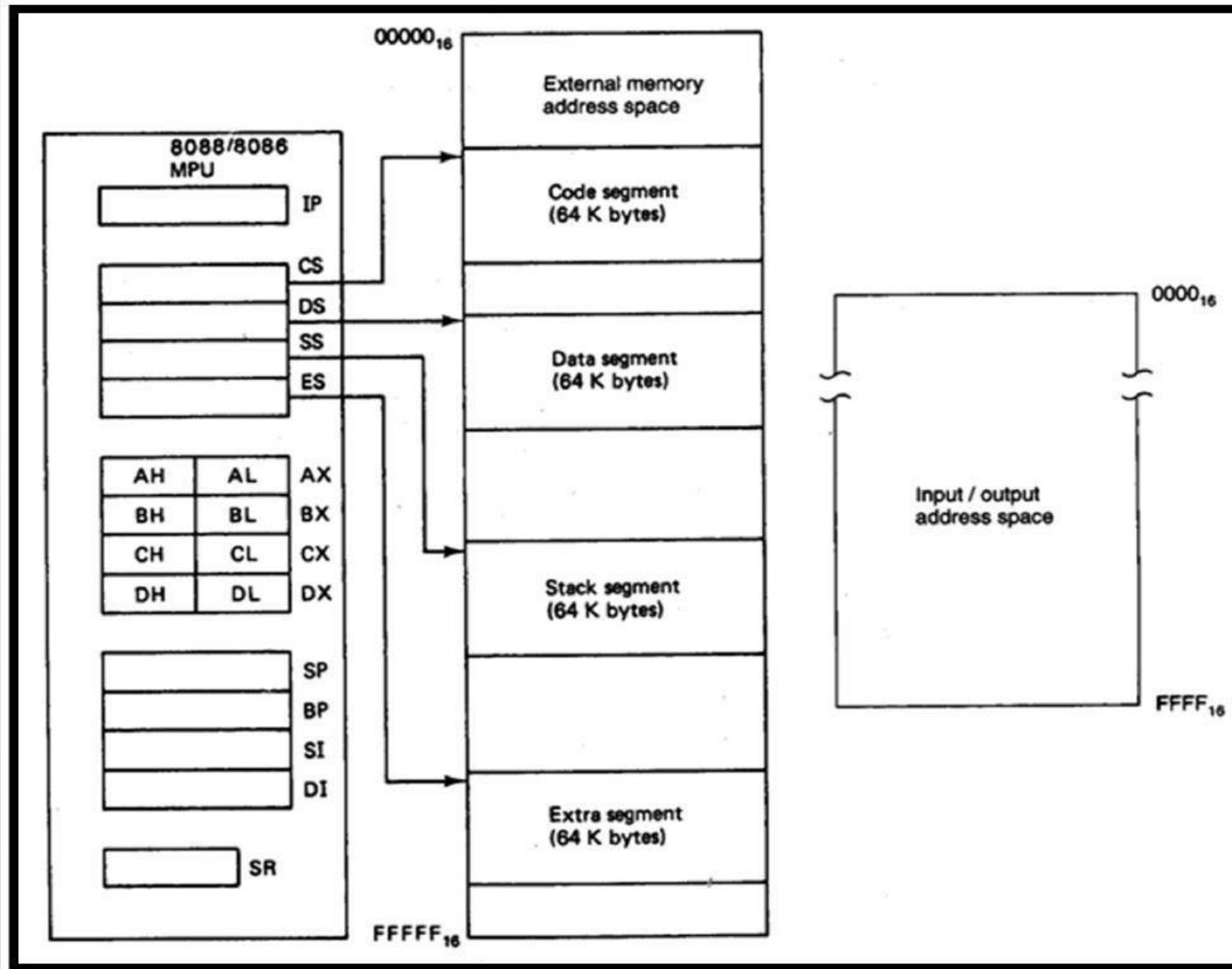
- **Code segment register (CS)** is used for addressing memory location in the code segment of the memory, where the executable program is stored.
- **Data segment register (DS)** is points to the data segment of the memory where the data is stored.
- **Extra segment register (ES)** also refers to a segment in the memory which is another data segment in the memory.
- **Stack segment register (SS)** is used for addressing stack segment of the memory. The stack segment is that segment of memory which is used to store stack data.

# Segments, Segment Registers & Offset Registers

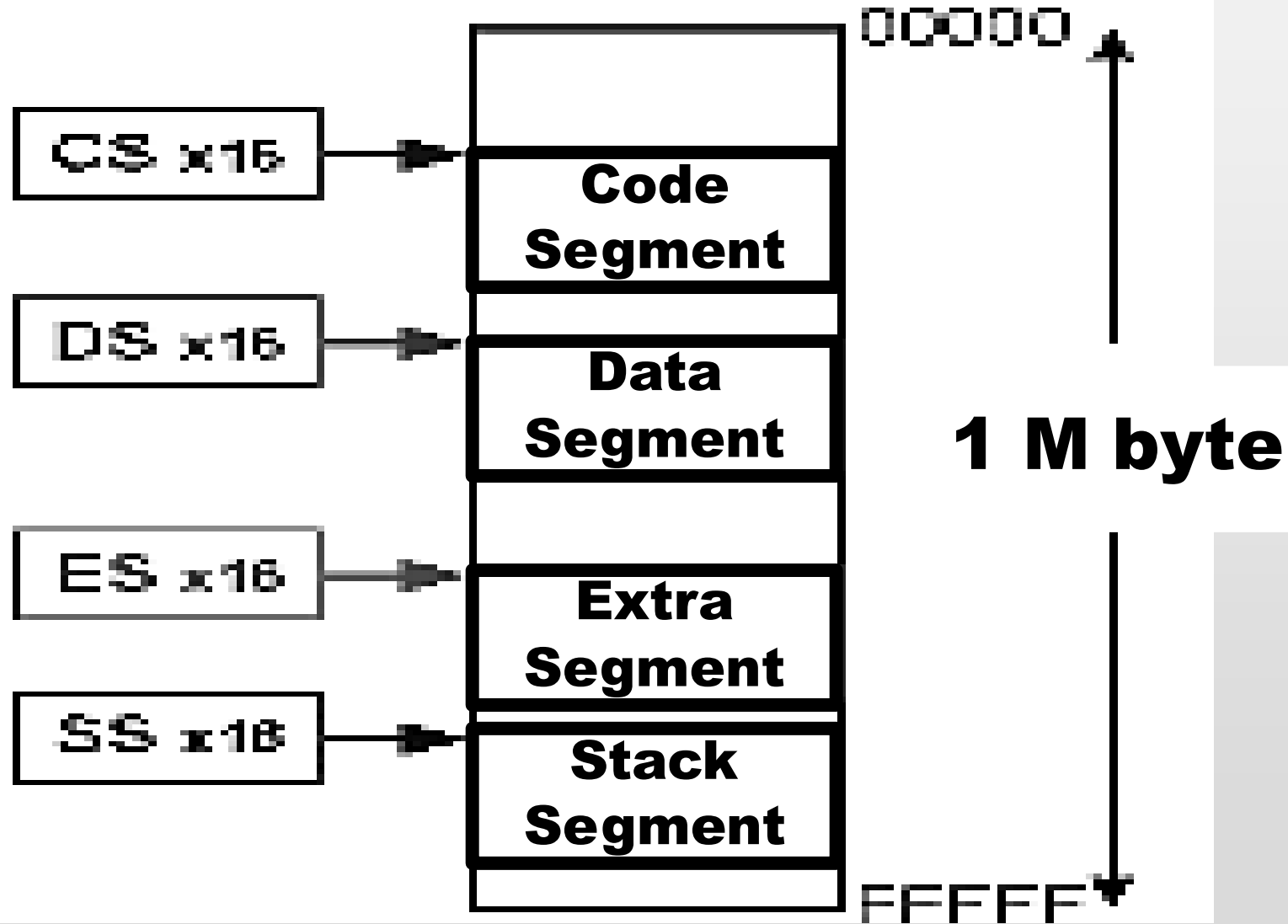
**The pointers contain offset within the particular segments.**

SEGMENT	SEGMENT REGISTER	OFFSET REGISTER
Code Segment	CSR	Instruction Pointer (IP)
Data Segment	DSR	Source Index (SI)
Extra Segment	ESR	Destination Index (DI)
Stack Segment	SSR	Stack Pointer (SP) / Base Pointer (BP)

# Block diagram showing software of 8086 or registers and memory



# Segment register



In Intel literature concerning the 8086, there are three types of addresses mentioned frequently: the physical address, the offset address, and the logical address.

**The physical address** is the 20-bit address that is actually put on the address pins of the 8086 microprocessors and decoded by the memory interfacing circuitry. This address can have a range of 00000H to FFFFFH for the 8086. This is an actual physical location in RAM or ROM within the 1 megabyte memory range.

**Physical address (PA) = Segment Address \* 10H + Offset Address**



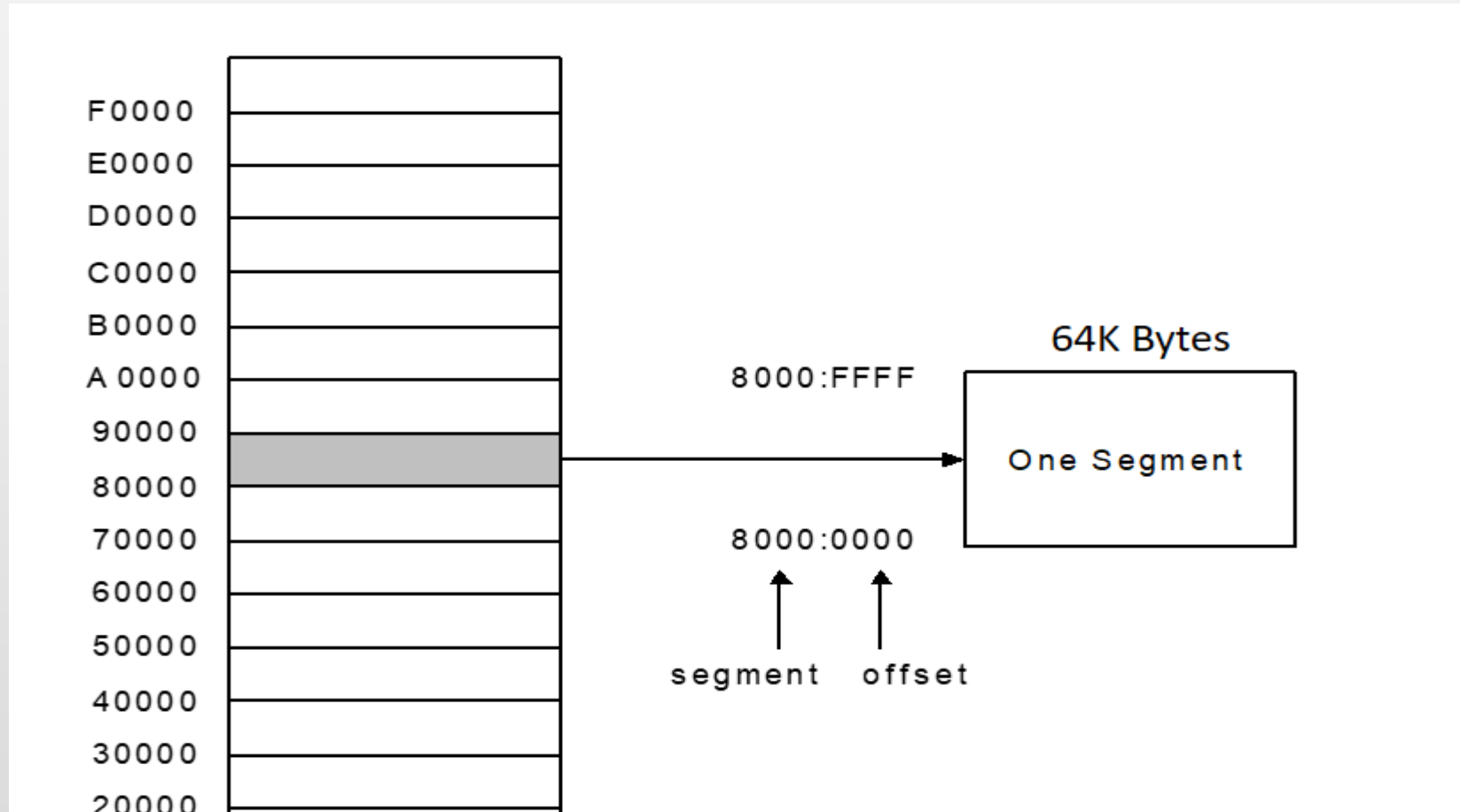
**CS, DS, ES, SS**



**IP, SI, DI, SP, BP**

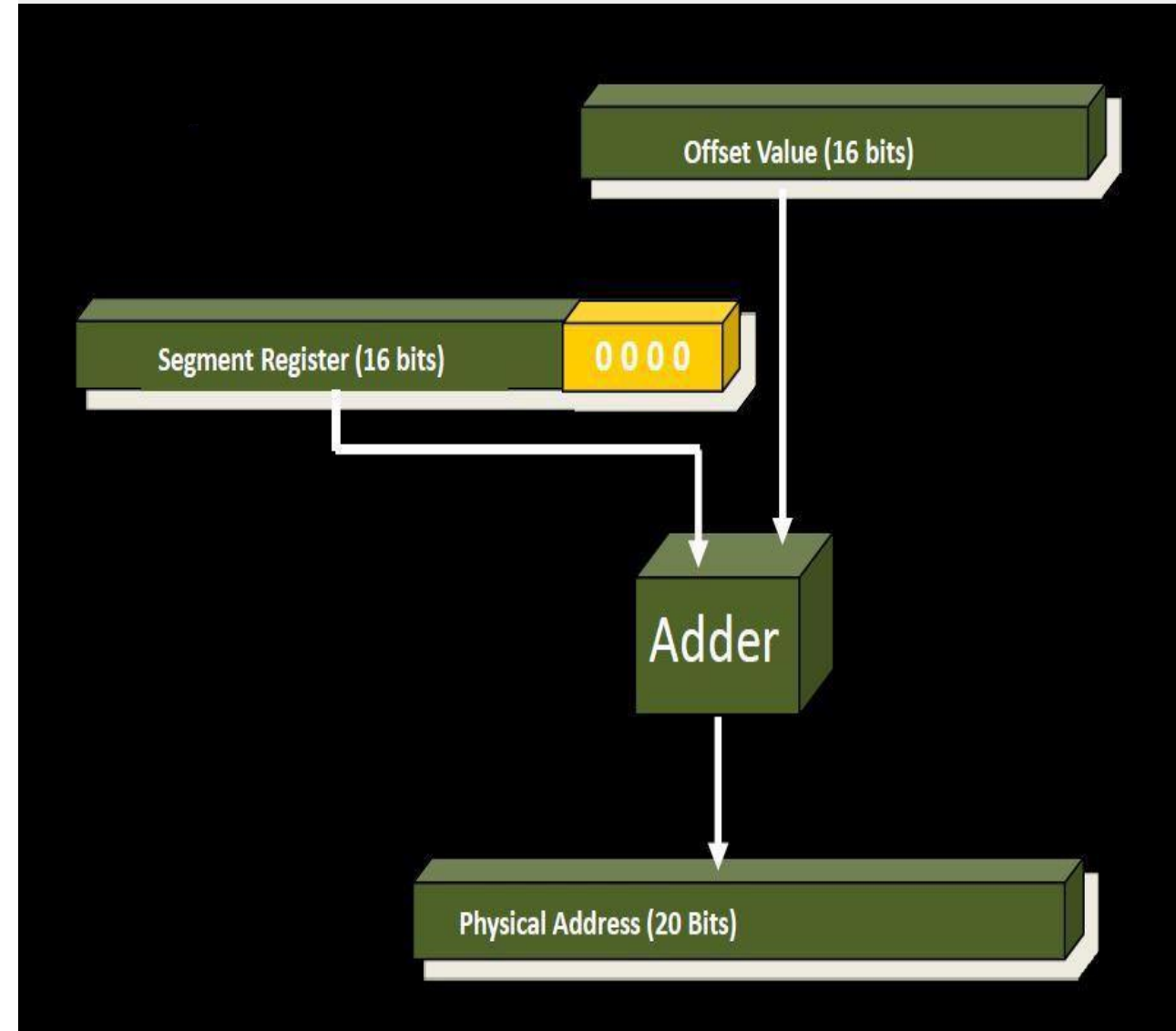
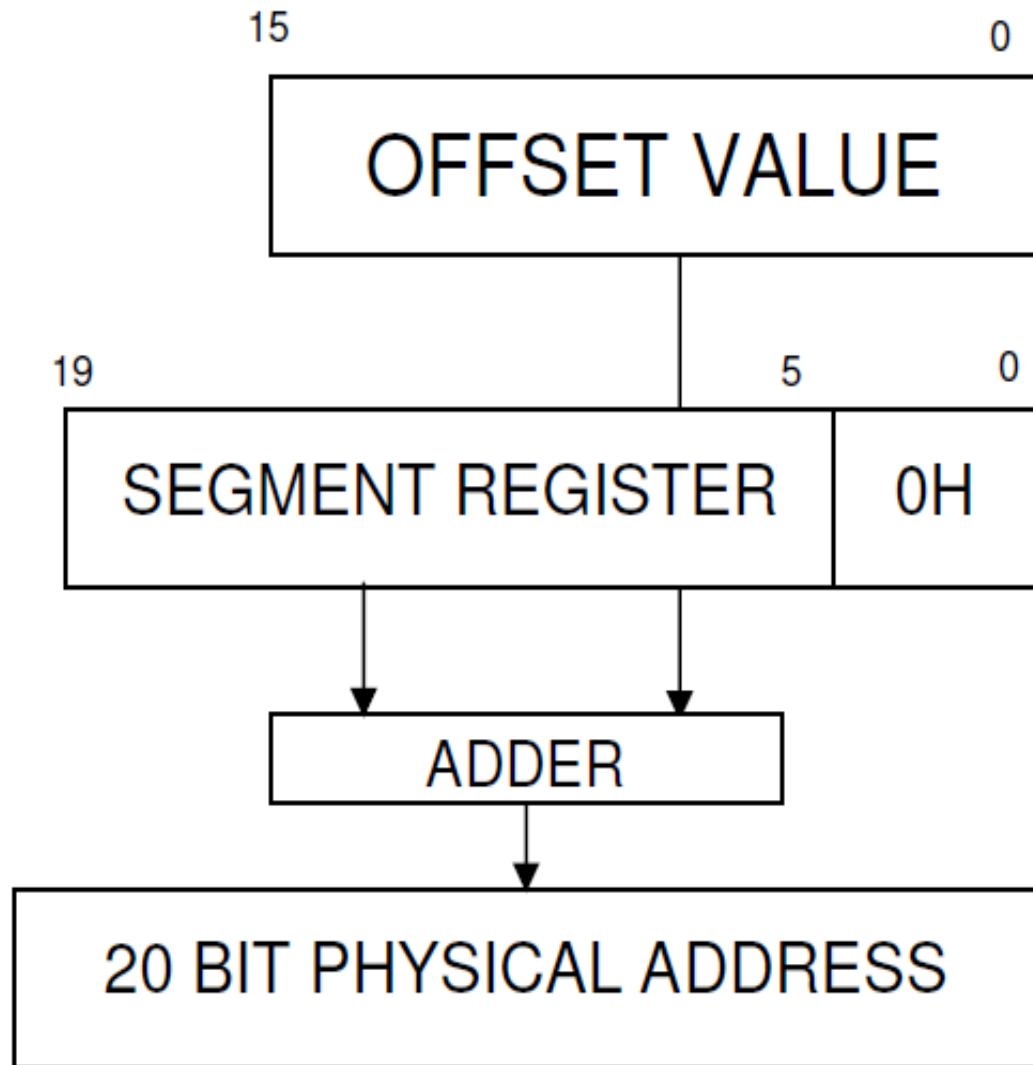


**The offset address** is a location with a 64K-byte segment range. There, an offset address can range from 0000H to FFFFH.



**The logical address** of an instruction always consists of a CS (code segment) and an IP (instruction pointer), shown in CS: IP format. Where CS is a segment and IP is an offset.

# Block diagram showing the segmentation



## Example 1

**The Contents of the following registers are :**

**CS = 1181H**

**DS = 3333H**

**SS = 2520H**

**IP = 1432H**

**SP = 1100H**

**DI = 0030H**

**SI = 1500H**

**Calculate the corresponding Physical Addresses for the address bytes in CS, DS and SS.**

## **Solution :**

**1.                    CS = 1181H            IP = 1432H**

**Physical address (PA) = Segment Address \*10H + Offset Address**



**CS, DS, ES, SS**



**IP, SI, DI, SP, BP**

**Physical address (PA) = CS\*10H + IP**

**Physical address (PA) = 1181H\*10H + 1432H**

**Physical address (PA) = 11810H + 1432H**

**Physical address (PA) = 12C42H**

**2.**                      **DS = 3333H**                      **SI = 1500H**

**Physical address (PA) = Segment Address \* 10H + Offset Address**



**CS, DS, ES, SS**



**IP, SI, DI, SP, BP**

**Physical address (PA) = DS \* 10H + SI**

**Physical address (PA) = 3333H \* 10H + 1500H**

**Physical address (PA) = 33330H + 1500H**

**Physical address (PA) = 34830H**

**3.**                      **SS = 2520H**                      **SP = 1100H**

**Physical address (PA) = Segment Address \* 10H + Offset Address**



**CS, DS, ES, SS**



**IP, SI, DI, SP, BP**

**Physical address (PA) = SS \* 10H + SP**

**Physical address (PA) = 2520H \* 10H + 1100H**

**Physical address (PA) = 25200H + 1100H**

**Physical address (PA) = 26300H**

## Example 2

CS

IP

2	5	0	0
---	---	---	---

 : 

9	5	F	3
---	---	---	---

1. Start with CS.

2	5	0	0
---	---	---	---

2. Shift left CS.

2	5	0	0	0
---	---	---	---	---

3. Add IP.

2	E	5	F	3
---	---	---	---	---

## Example 3

If **CS** = **24F6H** and **IP** = **634AH**, show:

- (a) The logical address.
- (b) The offset address.
- (c) The physical address.
- (d) The lower range.
- (e) The upper range of the code segment.

**Solution :**

(a) **24F6:634A**

(b) **634A**

(c)  **$24F60 + 634A = 2B2AA$**

(d)  **$24F60 + 0000 = 24F60$**

(e)  **$24F60 + FFFF = 34F5F$**



# Homework 1

**Q1 / The Contents of the following registers are :**

**CS = 4678H**

**DS = 5890H**

**SS = 3567H**

**ES = 2500H**

**IP = 4789H**

**BP = 2678H**

**DI = 0030H**

**SI = 5634H**

**Calculate the corresponding Physical Addresses for the address bytes in CS, DS, SS and ES.**

## Homework 2

**Q2 / If DS = 44F5H and SI = 745AH, show:**

- a) The logical address.**
- b) The offset address.**
- c) The physical address.**
- d) The lower range.**
- e) The upper range of the Data segment.**